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ABSTRACT:

PROBLEM TO BE SOLVED: To improve the yield of a wafer, based on impurity contamination by eliminating the effects of the impurity contamination with respect to a wafer.

SOLUTION: A surface of a semiconductor jig 14, wherein an SiC film 14b is formed by a CVD method in a surface of a substrate 14a formed of high purity carbon, for example is polished by a polishing jig 21, wherein an SiC film 21b is formed in a surface similarly. SiC particle residue which is generated in the polishing process is subjected to high temperature oxidation treatment and is removed by cleaning, such as HF. By applying this process for treatment of

a wafer mounting surface of a vertical wafer boat, it is possible to make a maximum surface roughness Rmax. of at most 10 μm in an n-time measurement in the measurement of L×n≥100 mm in surface roughness measurement, when measurement length is L mm and measurement frequency is (n) and to make the number of particles of 0.1 μm or more attaching to the surface at most 10 pieces/mm<SP>2</SP>. Thereby, a proper surface supporting of a wafer can be assured, and effects of impurity contamination to a wafer can be eliminated.

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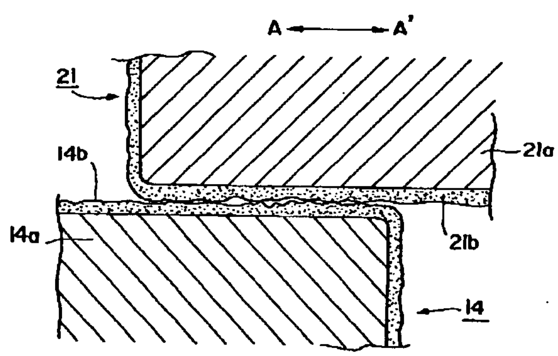
(54)【発明の名称】　半導体用治具およびその製造方法

(57)【要約】

【課題】　ウエハに対する不純物汚染の影響をなくし、不純物汚染に基づくウエハの歩留を向上し得るようにすること。

【解決手段】　例えば、高純度カーボンなどより成る基体１４ａの表面にＣＶＤ法によりＳｉＣ膜１４ｂを形成した半導体用治具１４の表面を、同様に表面にＳｉＣ膜２１ｂを形成した研摩治具２１により研摩する。この研摩工程により生成された残留ＳｉＣパーティクルは、高温酸化処理され、ＨＦ等の洗浄により除去される。これを縦型ウエハボートのウエハ積載面の処理に利用することで、測定長さ：Ｌｍｍ、測定回数：ｎとした際の表面粗さ測定におけるＬ×ｎ≧１００ｍｍの測定で、最大表面粗さＲｍａｘ．が前記ｎ回の測定で常に１０μｍ以下であり、かつ当該表面に付着する０．１μｍ以上のパーティクル数が１０個／ｍｍ²以下にすることができる。これにより、ウエハの適正な面支持が保証され、またウエハに対する不純物汚染の影響をなくすことができる。



1

【特許請求の範囲】

【請求項１】　基体表面にＣＶＤ法によりＳｉＣ膜を形成した半導体用治具であって、

測定長さ：Ｌｍｍ、測定回数：ｎとした際の表面粗さ測定におけるＬ×ｎ≧１００ｍｍの測定で、最大表面粗さＲｍａｘ．が前記ｎ回の測定で常に１０μｍ以下であり、かつ当該表面に付着する０．１μｍ以上のパーティクル数が１０個／ｍｍ^2 以下に成されていることを特徴とする半導体用治具。

【請求項２】　基体表面にＣＶＤ法によりＳｉＣ膜を形成した半導体用治具の製造方法であって、

基体表面にＣＶＤ法により形成されたＳｉＣ膜を、ＳｉＣ質の治具を使用して表面を平滑化する平滑化工程と、

前記平滑化工程を経た半導体用治具を高温酸素雰囲気中で熱処理し、平滑化工程によって生成され、治具の表面に付着したＳｉＣパーティクルをSiO_2 に転化させる熱処理工程と、

前記熱処理工程により転化されたSiO_2 を、溶解可能な溶液により洗浄する洗浄工程から成ることを特徴とする半導体用治具の製造方法。

【請求項３】　前記SiO_2 を溶解する溶液として、フッ酸またはフッ酸と塩酸、フッ酸と硝酸、フッ酸と硫酸のいずれかの混酸を用いたことを特徴とする請求項２に記載の半導体用治具の製造方法。

【請求項４】　前記ＳｉＣ質の治具は、含有金属不純物量が０．１ｐｐｍ以下に成されていることを特徴とする請求項２または請求項３に記載の半導体用治具の製造方法。

【請求項５】　ＣＶＤ法により基体表面に形成されたＳｉＣ膜を、ＳｉＣ質の治具を使用して平滑化させると共に、平滑化によって表面に付着したＳｉＣパーティクルを高温酸素雰囲気中でSiO_2 に転化し、このSiO_2 を溶解可能な溶液により洗浄して成ることを特徴とする半導体用治具。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体製造時の熱処理工程において使用される半導体用治具およびその製造方法に係り、特に縦型ウエハボートとその製造方法に関するものである。

【０００２】

【従来の技術】半導体製造工程における拡散工程等では熱処理炉が用いられ、半導体ウエハに対して高温の熱処理がなされる。この場合、周知のとおり半導体ウエハはウエハボートに載置された形で、高純度な石英ガラス等からなる炉芯管内に収納され、炉芯管内に熱処理用のガスを導入してウエハに対して所定の熱処理が施される。一方、近年の半導体の高集積化に伴いウエハの大口径化が進んでおり、これに伴い縦型ウエハボートが用いられる趨勢となっている。しかしながら支柱に溝部を形成

2

し、この溝部でウエハの端部を支持する形式の縦型ウエハボートを用いた場合には、ウエハの自重や面内温度差によりそれ自身にたわみが発生し、これに起因してウエハに対してスリップと呼ばれる結晶欠陥を発生させる原因となっている。

【０００３】そこで、ウエハボートのウエハ積載面を平面状に形成し、ウエハを面支持するようにして前記したようなウエハに対するスリップの発生を防止するようにした縦型ウエハボートが提案されている。ところで、このような縦型ウエハボートにおいては、従来その素材に石英ガラス材質が使用されていたが、近来においてはＣＶＤ（ｃｈｅｍｉｃａｌ　ｖａｐｏｒ　ｄｐｏｓｉｔｉｏｎ）法により基体にＳｉＣ膜を被覆すること（以下ＣＶＤ－ＳｉＣと称する。）により高純度化が達成できること、また耐熱性に優れることなどの理由から反応焼結ＳｉＣ質が使用されるようになってきた。

【０００４】

【発明が解決しようとする課題】しかしながら、ＣＶＤ－ＳｉＣ膜を被覆した反応焼結ＳｉＣ質の縦型ウエハボート（以下これをＣＶＤボートと称する）には、以下のような技術的な課題が存在している。先ず第１に、ＣＶＤ－ＳｉＣ膜は気相反応により形成される。この際、気相中でのＳｉＣ粒子の異常成長を１００％回避することができず、その内のいくつかの粒子が、ＣＶＤボートのウエハ積載面に堆積し、当該積載面で異常突起となる。第２に、ＣＶＤ反応管中に浮遊するゴミや、粒子がＣＶＤ反応前や反応中にＣＶＤボートのウエハ積載面に付着し、それらにＳｉＣ膜が選択的に形成され、当該積載面で異常突起となる。第３に、異常突起の生成を極力避けるようなＣＶＤ条件を選択すると、ＣＶＤ－ＳｉＣ膜を構成する結晶が粗大化し、表面の凹凸が顕著となる。

【０００５】前記した諸要因により、ウエハ積載面に生成される異常突起あるいは凹凸により、ウエハの裏面にはスリップと称される欠陥が発生することが知られている。前記スリップの発生は、特に酸化、拡散などの高温熱処理工程で顕著であり、熱処理ウエハの歩留を低下させる最大の要因となる。発明者らの実験計測によると、測定長さ：Ｌｍｍ、測定回数：ｎとした際の表面粗さ測定におけるＬ×ｎ≧１００ｍｍの測定で、最大表面粗さＲｍａｘ．が前記ｎ回の測定で１０μｍを越える状況においては、ウエハに発生するスリップが極端に増大することが確認された。これは、ウエハは積載面において、実質的に面支持ではなく点支持されることになり、ウエハの裏面部における前記点支持部において過大な負荷がウエハ面に集中するためであると考えられる。

【０００６】そこで、ウエハ積載面のＲｍａｘ．を低減させる手法として、発明者らはＣＶＤ膜で被覆されたウエハ積載面をダイヤモンド砥石などで機械加工し平滑化する方法なども検討したが、このような治具で加工することは、機械加工用治具からの不純物汚染が発生し、前

記したウエハの酸化、拡散などの高温熱処理工程でウエハに対して不良を発生させるという技術的課題が発生した。さらに、加工時に生成した1μm以下のパーティクルがウエハ積載面に吸着してしまい、工程内でのパーティクル源となり、別な意味で熱処理時でのウエハの歩留を下げてしまうという技術的課題が発生した。

【0007】本発明は前記したような技術的課題を解決するためになされたものであり、ウエハに対する不純物汚染の影響をなくし、不純物汚染に基づくウエハの歩留を向上し得る半導体用治具およびその製造方法を提供することを目的とするものである。また本発明はウエハ積載面を平面状とした縦型ウエハボートに適用した場合において、ウエハ積載面における平面性を改善して、ウエハに対するスリップの発生を低減し、またウエハ積載面の平面処理の処理効率を向上し得る縦型ウエハボートおよびその製造方法を提供することを目的とするものである。

【0008】

【課題を解決するための手段】前記課題を解決するためになされた本発明にかかる半導体用治具は、基体表面にＣＶＤ法によりＳｉＣ膜を形成した半導体用治具であって、測定長さ：Ｌmm、測定回数：ｎとした際の表面粗さ測定における$L \times n \geq 100$mmの測定で、最大表面粗さＲｍａｘ．が前記ｎ回の測定で常に10μm以下であり、かつ当該表面に付着する0．1μm以上のパーティクル数が10個／mm^2 以下に成されていることを特徴とする。なお、前記測定長さおよび測定回数は、被測定物である半導体用治具の種類および形状により適宜選択すればよいが、測定精度を考慮すると、測定回数は5回以上が好ましく、より好ましくは10回以上である。

【0009】また、本発明にかかる半導体用治具の製造方法は、基体表面にＣＶＤ法によりＳｉＣ膜を形成した半導体用治具の製造方法であって、基体表面にＣＶＤ法により形成されたＳｉＣ膜を、ＳｉＣ質の治具を使用して表面を平滑化する平滑化工程と、前記平滑化工程を経た半導体用治具を高温酸素雰囲気中で熱処理し、平滑化工程によって生成され、治具の表面に付着したＳｉＣパーティクルをSiO_2に転化させる熱処理工程と、前記熱処理工程により転化されたSiO_2 を、溶解可能な溶液により洗浄する洗浄工程とが具備される。そして、好ましくは前記SiO_2 を溶解する溶液として、フッ酸またはフッ酸と塩酸、フッ酸と硝酸、フッ酸と硫酸のいずれかの混酸が用いられる。また、好ましくは前記ＳｉＣ質の治具は、含有金属不純物量が0．1ppm以下のものが使用される。

【0010】さらに本発明にかかる半導体用治具は、ＣＶＤ法により基体表面に形成されたＳｉＣ膜を、ＳｉＣ質の治具を使用して平滑化させると共に、平滑化によって表面に付着したＳｉＣパーティクルを高温酸素雰囲気中でSiO_2 に転化し、このSiO_2 を溶解可能な溶液

により洗浄してなることを特徴とする。

【0011】以上のように成された半導体用治具およびその製造方法によると、例えば反応焼結炭化珪素（以下、Ｓｉ－ＳｉＣと記す）などの基体表面に対して先ずＣＶＤ法によりＳｉＣ膜が形成される。そして基体表面に形成されたＳｉＣ膜は、ＣＶＤボートの被覆膜と同材質のＣＶＤ－ＳｉＣ質により研摩され、平滑化される。この研摩、平滑化によって生じたＳｉＣのパーティクルは、高温下の酸素気流中で熱処理が成され、これによりＳｉＣのパーティクルは全てSiO_2 に転化される。このようにして転化されたSiO_2 は、ＨＦ（フッ酸）系の溶液により洗浄することで、残留パーティクルを極端に低減させることができる。

【0012】この場合、前記基体表面に形成されたＳｉＣ膜を研摩するためのＣＶＤ－ＳｉＣ質の治具は、含有金属不純物量が0．1ppm以下に管理することで、実用上の不純物汚染による影響は少ないことが判明した。この製造方法を半導体治具としての縦型ウエハボートのウエハ積載面に適用することで、測定長さ：Ｌmm、測定回数：ｎとした際の表面粗さ測定における$L \times n \geq 100$mmの測定で、最大表面粗さＲｍａｘ．が前記ｎ回の測定で常に10μm以下であり、かつ当該表面に付着する0．1μm以上のパーティクル数が10個／mm^2 以下とすることができる。そして、このようにして形成された縦型ウエハボートによると、その積載面に積載されたウエハは実質的に面支持状態を確保することができ、ウエハに対するスリップの発生を効果的に低減させることが可能となる。

【0013】

【発明の実施の形態】本発明にかかる半導体用治具およびその製造方法について、半導体用治具として縦型ウエハボートにこれを適用した実施の形態に基づいて説明する。図1は縦型ウエハボート10の基本形態を示したものである。すなわち、複数本の支柱11の上下両端部には天盤12と底盤13とが位置しており、これらの間には複数の支持盤14が所定の挿入空間をもって配置されている。そして、天盤12と底盤13、および各支持盤14は前記複数の支柱11に設けられた溝部に設置されている。また前記各支持盤14には、スリット15が形成されており、このスリット15が形成された各支持盤14の上面は、ウエハ16の積載面を形成している。

【0014】図2は前記した支持盤14の一部を断面状態とし、支持盤14のウエハ積載面に対して処理を施す状態を示したものである。支持盤14を構成する基体14ａは、例えばＳｉ－ＳｉＣにより形成されており、この基体14ａの表面にはＣＶＤ法によりＳｉＣ膜14ｂが形成されている。そして、支持盤14のウエハ積載面における前記ＳｉＣ膜14ｂの表面は、研摩治具21により研摩される。前記研摩治具21は、例えば高純度カーボンよりなる基体21ａの表面にＣＶＤ法によりＳｉ

C膜２１ｂが形成されている。そして前記研摩治具２１（以下、これをＳｉＣ治具ともいう）を、図２の矢印Ａ－Ａ′方向に往復動させるか、または水平方向に回転駆動させることにより、支持盤１４のウエハ積載面における前記ＳｉＣ膜１４ｂの表面は、研摩治具２１により研摩され平滑化される。

【００１５】前記のように、支持盤１４および研摩治具２１のいずれにおいても、基体の表面にＣＶＤ法によりＳｉＣ膜を形成させることで、その特質としてＳｉＣ膜は超高純度であり、不純物汚染の問題が発生することがない。またＳｉＣはダイヤモンドなどに次ぐ高い硬度を有するものであるため、その研摩効率を向上させることができる。このようにして、その表面が平滑化された支持盤１４には、結果として支持盤１４の表面を被覆するＳｉＣおよび研摩治具２１の表面を被覆するＳｉＣがパーティクルとなって残留することとなる。このようにして残留するパーティクルはウエハ積載面に多量に付着し、ウエハ熱処理時の炉内パーティクル源となる問題が生ずる。

【００１６】この対策として、加工後のＣＶＤボートを超純水中で超音波洗浄、煮沸洗浄したり、ＨＦ溶液中に浸漬したが、サブミクロンオーダーのパーティクルはほとんど除去できないことが判明した。ここで発明者らは、ＳｉＣによるパーティクルを除去するために、次の＊

＊ような手段を開発した。すなわち図２に示したように研摩治具２１によるウエハ積載面の平滑化加工が完了したウエハボート１０を高温下、酸素気流中で熱処理をおこなった。これは下記反応式（化１）によりＳｉＣをSiO_2 に変化させるためである。したがって、所定時間熱処理をおこなえば、ＳｉＣのパーティクルは全てSiO_2 に変化することになる。

【００１７】

【化１】$2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO$

【００１８】前記熱処理により転換されたSiO_2 は、ＨＦ（フッ酸）系の溶液に容易に反応し、溶解してしまうことが知られている。そこで、酸素気流中で熱処理をおこなったボート１０をＨＦ溶液中に浸漬させた。この結果、SiO_2 化したパーティクルは全てＨＦ溶液中に溶解してしまい、ウエハ積載面には０．１μｍ以上のパーティクル数が１０個／mm^2 以下に低減していることが確認された。またこれは、半導体製造用の熱処理工程で十分できるレベルであることも併せて確認した。

【００１９】

【実施例】同一形状の８″ＣＶＤボートを２２台作製して、表１に示した１１通りの後処理をおこなったウエハボートを２台づつ準備した。

【００２０】

【表１】

No.	後処理内容
1	未処理（リファレンス）
2	ウエハ積載面を既存の治具（ダイヤモンド）で機械加工実施
3	ウエハ積載面を高純度SiC治具で加工実施
4	No.2処理後、ボートの超音波洗浄実施
5	No.2処理後、ボートの煮沸洗浄実施
6	No.2処理後、ボートのフッ酸洗浄実施
7	No.3処理後、ボートの超音波洗浄実施
8	No.3処理後、ボートの煮沸洗浄実施
9	No.3処理後、ボートのフッ酸洗浄実施
10	No.2処理後、ボートを酸素気流中で熱処理し、更にフッ酸洗浄実施
11	No.3処理後、ボートを酸素気流中で熱処理し、更にフッ酸洗浄実施

（注記：No.１１が本発明品に相当する。）

【００２１】まず、はじめに各１台を破壊し、ウエハ積載面のＲｍａｘ．とパーティクル（０．１～１μｍ）の付着状況を調査した。Ｒｍａｘ．は、触針式表面粗さ計（東京精密：ＳＵＲＦＣＯＭ）で測定し、パーティクルの付着状況は電子顕微鏡（ＳＥＭ）で観察した。結果を表２に示した。なお、この場合のＲｍａｘ．の測定条件は、測定長さ：１０mm、カットオフ値：０．８mm、※

※走査速度：０．３mm／ｓｅｃ、繰り返し測定回数：１０回とした。Ｒｍａｘ．は加工時間などによって若干ばらつきが認められたものの、本発明に相当するボートＮｏ．１１は、Ｒｍａｘ．が低値で推移し、かつ付着しているパーティクルもＮｏ．１（比較例）並に少ないことが確認された。

【００２２】

【表２】

No.	Rmax.(μm)	パーティクルの付着状況（ヶ／mm^2）
1	8.0～35.0	0～ 5
2	5.5～12.2	100以上
3	5.8～13.5	100以上
4	2.2～ 7.8	100以上
5	2.3～ 7.7	100以上
6	2.1～ 7.9	100以上
7	3.6～ 9.0	100以上
8	3.7～ 8.9	100以上
9	3.5～ 9.2	100以上
10	2.0～ 7.2	20～80
11	3.2～ 8.1	0～ 4

（注記：No. １１が本発明品に相当する。）

【００２３】また、前記Ｎｏ．１（比較例）と、本発明に相当するボートＮｏ．１１についての各回のＲｍａｘ．の実測データを含む詳細な測定結果を表３に示す。なお表３に示す測定データの単位はμｍである。表３から明らかなように、比較例は１０回の測定のうち、Ｒｍ＊ａｘ．で１０μｍを越えたものが６回であったのに対し、本発明品では１０回いずれでも、１０μｍ以下の値であり、「平均値＋３σ」でも１０μｍ以下で極めて表面が均等に滑らかになっているかが明らかである。

【００２４】

【表３】

測定数	比較例（No.1）	本発明（No.11）
1	9.5	7.2
2	12.4	5.7
3	35.0	5.4
4	8.0	3.2
5	21.7	6.5
6	10.4	5.6
7	11.2	4.9
8	9.3	8.1
9	29.2	4.6
10	8.8	4.3
平均値	15.55	5.55
標準偏差	9.64	1.44
平均値＋３σ	44.46	9.86
最小値	8.0	3.2
最大値	35.0	8.1

【００２５】ついで、非破壊のＣＶＤボートにウエハを積載し、酸化、拡散工程を想定した条件（１１００℃、酸素気流中、５時間）の熱処理をおこなつた。熱処理完了ウエハについて、

①スリップの発生状況

②ウエハ表面の不純物量（ＭＣＬ）

③ウエハ表面のパーティクル付着状況

について調査した。

前記①はウエハ裏面の斜光観察

※前記②はウエハ表面に形成された酸化膜中の不純物分析

前記③は光の散乱を利用したパーティクルカウンター測定で評価した。

その結果を表４にまとめた。なお、スリップの発生状況を示す表４における積算スリップ長は、ウエハ一枚の面内に存在するスリップ長さを全て加算した値である。Ｎｏ．１（比較例）と比較して、全ての項目において同等以上の好結果が得られたのは、不純物の少ないＳｉＣ治具を使用し、酸素気流中での熱処理を経た後にフッ酸洗

浄を実施したNo．11（本発明品）だけであつた。

【0026】

【表4】

No.	積算スリップ長	MCL : Fe	パーティクル数
	(mm／ウエハ)	($\times 10^{10}$atoms／cm^2)	(ヶ／ウエハ)
1	100～140	1.0	0～10
2	60～ 90	25.0	25～40
3	65～ 95	2.0	20～35
4	15～ 25	18.0	20～35
5	15～ 25	17.0	20～35
6	15～ 25	11.0	20～35
7	20～ 30	1.8	15～30
8	20～ 30	1.6	15～30
9	20～ 30	1.3	15～30
10	5～ 20	7.0	10～25
11	5～ 25	0.9	0～ 5

（注記：No.１１が本発明品に相当する。）

【００２７】ここで、ＳｉＣ治具、酸素気流中での熱処理条件、ＨＦ溶液中での洗浄条件の実施例について示す。ＳｉＣ治具は、前記のごとくＳｉ－ＳｉＣなどより成る基体にＣＶＤ－ＳｉＣ膜を形成し、最大表面粗さが２０～１００μm程度のものが好ましい。ＣＶＤ法以外で得られたＳｉＣ材料は、助剤や接着剤として不純物を含むため不適であり、最大表面粗さが前記範囲外であると加工効率が落ちたり、所定の面粗さが達成できなくなる。酸素気流中での熱処理条件は、少なくとも１１００℃以上であることが必要である、これは前記した反応式（化１）を効率良く進行させるためである。一般的に前記反応式（化１）における反応進行度合は、温度の関数であるとともに処理時間の平方根に比例する（放物線則）。

【００２８】これを基にすれば、１２５０℃の場合、処理時間を１５時間に設定すれば、１μm以下のＳｉＣパーティクルは全てＳｉＯ$_2$ に転化してしまう。１μm以上のパーティクルは表面に吸着しにくいため、特にＳｉＯ$_2$ 化させる必要はない。ＨＦ洗浄は、特に厳しく制御する因子は少なく、１０％以上の溶液に２時間以上ＣＶＤボートを浸漬せればＳｉＯ$_2$ パーティクルは完全に溶解してしまうことが確認された。

【００２９】なお、以上の実施の形態並びに実施例においては、ＳｉＯ$_2$ を溶解する溶液として、フッ酸を用いた例に基づいて説明したが、前記溶液としては、フッ酸と塩酸、フッ酸と硝酸、フッ酸と硫酸のいずれかの混酸を用いても、同等の洗浄効果が得られることが確認された。また、前記したＣＶＤ－ＳｉＣ質の治具は、含有金属不純物量が０．１ｐｐｍ以下に成されることにより、ウエハの酸化、拡散などの高温熱処理工程で金属不純物によりウエハに対して不良を発生させる度合いが低下できることも確認された。

【００３０】また図１においては、半導体用治具として天盤と底盤との間に複数枚のウエハ支持盤を備えた縦型ウエハボートを例示しているが、本発明はこのような特定な縦型ウエハボートに限らず、例えば４本の支柱に対してウエハ保持溝を備えた一般的なウエハボートに適用できることは勿論である。さらに本発明は枚葉式のサセプタ、ウエハ搬送用トレー等に対して適用することもでき、またそれ以外の例えば炉芯管などの半導体用治具に対して適用することができる。

【００３１】

【発明の効果】以上のように、本発明にかかる半導体用治具およびその製造方法によると、基体表面にＣＶＤ法によりＳｉＣ膜を形成し、このＳｉＣ膜をＳｉＣ膜を形成した研摩治具により平滑化し、続いて高温酸化処理、およびＨＦ等の洗浄の組合せによるパーティクル除去を行うようにしたので、その最大表面粗さが、１０μm以下の平滑化が可能となり、かつ不純物汚染やパーティクル発生も抑制することが可能となる。したがって、これを縦型ウエハボートのウエハ積載面の処理に適用することで、従来問題となっていたウエハのスリップの発生を抑制でき、処理ウエハの歩留向上に貢献することができる。なお上述した炉芯管等のようにウエハと直接接触しない半導体用治具においては、前記したスリップ抑制機能はないが、不純物汚染やパーティクル発生の抑制機能によって、処理ウエハの歩留向上に貢献することができる。

【図面の簡単な説明】

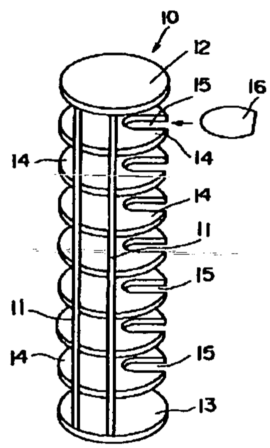
【図１】本発明にかかる半導体用治具としての縦型ウエハボートの例を示した斜視図である。

【図2】図1に示す縦型ウエハボートにおけるウエハ積載面を研摩処理する工程を示した拡大断面図である。

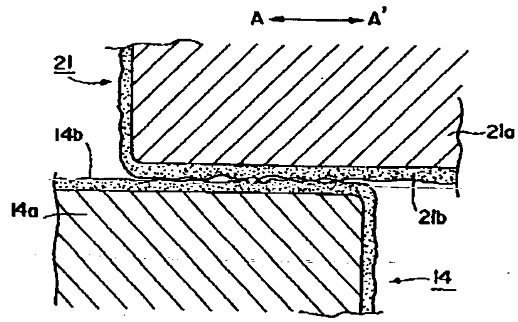
【符号の説明】

10　縦型ウエハボート
11　支柱
12　天盤
13　底盤
14　支持盤
14a　基体
14b　SiC膜
15　スリット
16　ウエハ
21　研摩治具
21a　基体
21b　SiC膜

【図1】



【図2】



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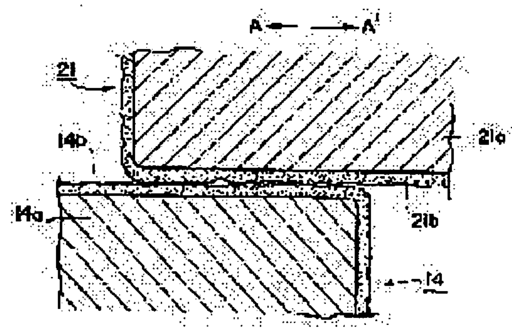
(54) SEMICONDUCTOR JIG AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To improve the yield of a wafer, based on impurity contamination by eliminating the effects of the impurity contamination with respect to a wafer.



SOLUTION: A surface of a semiconductor jig 14, wherein an SiC film 14b is formed by a CVD method in a surface of a substrate 14a formed of high purity carbon, for example is polished by a polishing jig 21, wherein an SiC film 21b is formed in a surface similarly. SiC particle residue which is generated in the polishing process is subjected to high temperature oxidation treatment and is removed by cleaning, such as HF. By applying this process for treatment of a wafer mounting surface of a vertical wafer boat, it is possible to make a maximum surface roughness Rmax. of at most 10 μm in an n-time measurement in the measurement of $L\times n\geq 100$ mm in surface roughness measurement, when measurement length is L mm and measurement frequency is (n) and to make the number of particles of 0.1 μm or more attaching to the surface at most 10 pieces/mm2. Thereby, a proper surface supporting of a wafer can be assured, and effects of impurity contamination to a wafer can be eliminated.

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the fixture for semiconductors used in the heat treatment process at the time of semiconductor manufacture, and its manufacture method, especially relates to a vertical-mold wafer boat and its manufacture method.
[0002]
[Description of the Prior Art] At the diffusion process in a semiconductor manufacturing process, a heat treating furnace is used and hot heat treatment is made to a semiconductor wafer. In this case, as everyone knows, a semiconductor wafer is contained in the reactor core tube which consists of high grade quartz glass etc. in the form laid in the wafer boat, introduces the gas for heat treatment in a reactor core tube, and predetermined heat treatment is performed to a wafer. On the other hand, diameter-ization of macrostomia of a wafer is progressing with high integration of a semiconductor in recent years, and it has become the trend for which a vertical-mold wafer boat is used in connection with this. However, a slot is formed in a support, and when the vertical-mold wafer boat of the form which supports the edge of a wafer in this slot is used, it is the cause of generating the crystal defect which a deflection occurs in itself by the self-weight of a wafer, or the temperature gradient within a field, originates in this, and is called slip to a wafer.
[0003] Then, the wafer loading side of a wafer boat is formed in a plane, and the vertical-mold wafer boat which prevented generating of a slip to a wafer which described the wafer above as carried out field support is proposed. By the way, in such a vertical-mold wafer boat, although the quartz-glass quality of the material was conventionally used for the material, the quality of reaction-sintering SiC has come to be used from the reasons of that high grade-ization can be attained, excelling in thermal resistance by covering a SiC film with the CVD (chemical vapor dposition) method to a base in these days (CVD-SiC being called below.).
[0004]
[Problem(s) to be Solved by the Invention] However, the following technical technical problems exist in the vertical-mold wafer boat (this is called a CVD boat below) of the quality of reaction-sintering SiC which covered the CVD-SiC film. A CVD-SiC film is first formed in the 1st of gaseous phase reaction. Under the present circumstances, unusual growth of the SiC particle in the inside of a gaseous phase is nonavoidable 100%, and some particles of them deposit on the wafer loading side of a CVD boat, and serve as an unusual salient in respect of the loading concerned. The dust which floats in a CVD coil, and a particle adhere a CVD reaction front and into a reaction in the wafer loading side of a CVD boat, a SiC film is alternatively formed in them, and it is set to the 2nd with an unusual salient in respect of the loading concerned. If CVD conditions which avoid generation of an unusual salient as much as possible are chosen as the 3rd, the crystal which constitutes a CVD-SiC film will turn big and rough, and surface irregularity will become remarkable.
[0005] In the rear face of a wafer, it is known with the unusual salient or irregularity generated by many of said factors in a wafer loading side that the defect called a slip will occur. Especially generating of the

aforementioned slip is remarkable at elevated-temperature heat treatment processes, such as oxidization and diffusion, and becomes the greatest factor which reduces the yield of a heat treatment wafer. According to artificers' experiment measurement, it was checked that the slip generated to a wafer in the situation that maximum surface roughness Rmax. exceeds 10 micrometers by n aforementioned measurement, in the measurement of Lxn>=100mm in the surface roughness measurement at the time of being referred to as measurement length:Lmm and measurement count:n increases extremely. It is thought that this is to field-support not but point support a wafer substantially in a loading side, and for an excessive load to concentrate on a wafer side in the aforementioned point supporter in the rear-face section of a wafer.

[0006] Then, although artificers examined how to machine the wafer loading side covered with the CVD film by the diamond wheel etc., and smooth etc. as the technique of reducing Rmax. of a wafer loading side The technical technical problem that processing it with such a fixture generated a defect to a wafer at elevated-temperature heat treatment processes, such as oxidization of the wafer which the impurity contamination from the fixture for machining generated and described above, and diffusion, occurred. Furthermore, the particle 1 micrometer or less generated at the time of processing stuck to the wafer loading side, it became a source of particle within a process, and the technical technical problem that the yield of the wafer in the time of heat treatment will be lowered in another meaning occurred.

[0007] It is made in order that this invention may solve a technical technical problem which was described above, and the influence of the impurity contamination to a wafer is lost, and it aims at offering the fixture for semiconductors which may improve the yield of a wafer based on impurity contamination, and its manufacture method. Moreover, this invention aims at offering the vertical-mold wafer boat which improves the smoothness in a wafer loading side, and reduces generating of a slip to a wafer, and may improve the processing efficiency of flat-surface processing of a wafer loading side, and its manufacture method, when a wafer loading side is applied to the vertical-mold wafer boat made into the plane.

[0008]

[Means for Solving the Problem] The fixture for semiconductors concerning this invention made in order to solve the aforementioned technical problem By the measurement of Lxn>=100mm in the surface roughness measurement at the time of being the fixture for semiconductors which formed the SiC film in the base front face by CVD, and being referred to as measurement length:Lmm and measurement count:n The number of particle of 0.1 micrometers or more which maximum surface roughness Rmax. is always 10 micrometers or less in n aforementioned measurement, and adheres to the front face concerned is 2 ten pieces/mm. It is characterized by having accomplished below. In addition, although what is necessary is just to choose the aforementioned measurement length and a measurement count suitably with the kind and configuration of the fixture for semiconductors which are a device under test, when the accuracy of measurement is taken into consideration, 5 times or more of a measurement count are desirable, and it is 10 times or more more preferably.

[0009] Moreover, the manufacture method of the fixture for semiconductors concerning this invention The smoothing process which smooths a front face for the SiC film which is the manufacture method of the fixture for semiconductors which formed the SiC film in the base front face by CVD, and was formed in the base front face of CVD using the fixture of the quality of SiC, The heat treatment process which makes the SiC particle which heat-treated the fixture for semiconductors which passed through the aforementioned smoothing process in elevated-temperature oxygen atmosphere, was generated by the smoothing process, and adhered on the surface of the fixture convert into SiO2, SiO2 converted by the aforementioned heat treatment process The washing process washed with the solution which can dissolve possesses. And it is the above SiO2 preferably. As a dissolving solution, the mixed acid of fluoric acid or fluoric acid, a hydrochloric acid and fluoric acid, a nitric acid and fluoric acid, or a sulfuric acid is used. Moreover, as for the fixture of the aforementioned quality of SiC, a thing 0.1 ppm or less is preferably used for the content metal impure amount of resources.

[0010] The fixture for semiconductors furthermore applied to this invention is the SiC particle which adhered to the front face by smoothing while carrying out smoothing of the SiC film formed in the base

front face of CVD using the fixture of the quality of SiC in elevated-temperature oxygen atmosphere SiO_2 It converts and is this SiO_2. The solution which can dissolve washes and it is characterized by the bird clapper.

[0011] According to the fixture for semiconductors accomplished as mentioned above, and its manufacture method, a SiC film is first formed of CVD, for example to base front faces, such as a reaction-sintering silicon carbide (it is hereafter described as Si-SiC). And the SiC film formed in the base front face is polished by the quality of CVD-SiC of the covering film of a CVD boat, and this quality of the material, and smoothing is carried out. Heat treatment accomplishes the particle of SiC produced by this polishing and smoothing in the oxygen air current under an elevated temperature, and, thereby, all the particle of SiC is SiO_2. It is converted. Thus, converted SiO_2 By washing with the solution of HF (fluoric acid) system, remains particle can be reduced extremely.

[0012] In this case, the fixture of the quality of CVD-SiC for polishing the SiC film formed in the aforementioned base front face is that the content metal impure amount of resources manages to 0.1 ppm or less, and the few thing made the influence by practical impurity contamination clear. The number of particle of 0.1 micrometers or more which maximum surface roughness Rmax. is always 10 micrometers or less in n aforementioned measurement, and adheres to the front face concerned in the measurement of Lxn>=100mm in the surface roughness measurement at the time of being referred to as measurement length:Lmm and measurement count:n by applying this manufacture method to the wafer loading side of the vertical-mold wafer boat as a semiconductor fixture is 2 ten pieces/mm. It can consider as the following. And according to the vertical-mold wafer boat formed by doing in this way, the wafer loaded into the loading side can secure a field support state substantially, and it becomes possible to reduce generating of a slip to a wafer of it effectively.

[0013]

[Embodiments of the Invention] The fixture for semiconductors concerning this invention and its manufacture method are explained to a vertical-mold wafer boat based on the gestalt of the operation which applied this as a fixture for semiconductors. Drawing 1 shows the basic gestalt of the vertical-mold wafer boat 10. That is, the roof 12 and the batholith 13 are located in the vertical both ends of two or more supports 11, and two or more support boards 14 are arranged with predetermined insertion space among these. And a roof 12, a batholith 13, and each support board 14 are installed in the slot established in two or more aforementioned supports 11. Moreover, the upper surface of each support board 14 in which the slit 15 is formed in and this slit 15 was formed forms the loading side of a wafer 16 in each aforementioned support board 14.

[0014] Drawing 2 makes a part of said support board 14 a cross-section state, and the state of processing to the wafer loading side of the support board 14 is shown. Base 14a which constitutes the support board 14 is formed of Si-SiC, and SiC film 14b is formed in the front face of this base 14a of CVD. And the front face of the aforementioned SiC film 14b in the wafer loading side of the support board 14 is polished by the polishing fixture 21. SiC film 21b is formed in the front face of base 21a on which the aforementioned polishing fixture 21 consists for example, of high grade carbon of CVD. And by making it reciprocate in the direction of arrow A-A' of drawing 2 , or carrying out the rotation drive of the aforementioned polishing fixture 21 (this also being hereafter called SiC fixture) horizontally, the front face of the aforementioned SiC film 14b in the wafer loading side of the support board 14 is polished by the polishing fixture 21, and smoothing is carried out.

[0015] As mentioned above, in any of the support board 14 and the polishing fixture 21, as the special feature, a SiC film is a super-high grade and the problem of impurity contamination does not generate it by making a SiC film form by CVD on the surface of a base. Moreover, since SiC is what has the high degree of hardness which ranks second to a diamond etc., it can raise the polishing efficiency. Thus, to the support board 14 to which smoothing of the front face was carried out, SiC which covers the front face of SiC which covers the front face of the support board 14 as a result, and the polishing fixture 21 serves as particle, and will remain. Thus, the particle which remains adheres to a wafer loading side so much, and the problem used as the source of the particle in a furnace at the time of wafer heat treatment produces it.

[0016] As this cure, the CVD boat after processing was cleaned ultrasonically in ultrapure water, and although boiling washing was carried out or it was immersed into HF solution, that it is hardly unremovable made the particle of submicron order clear. Artificers developed the following meanses here, in order to remove the particle by SiC. That is, the wafer boat 10 which smoothing processing of the wafer loading side by the polishing fixture 21 completed as shown in drawing 2 was heat-treated under an elevated temperature and in the oxygen air current. This is SiC by the following reaction formula (** 1) SiO2 It is for making it change. Therefore, if predetermined-time heat treatment is performed, all the particle of SiC will be SiO2. It will change.
[0017]
[Formula 1] 2SiC+3O2 ->2SiO2+2CO[0018] SiO2 converted by the aforementioned heat treatment Reacting to the solution of HF (fluoric acid) system easily, and dissolving in it is known. Then, the boat 10 which heat-treated in the oxygen air current was made immersed into HF solution. Consequently, SiO2 For all the particle that turned, it dissolves into HF solution and the number of particle of 0.1 micrometers or more is 2 ten pieces/mm in a wafer loading side. Decreasing below was checked. Moreover, this also checked collectively that it was the level made enough at the heat treatment process for semiconductor manufacture.
[0019]
[Example] It prepared at a time two wafer boats which performed 11 kinds of the same configuration which-produced-8" of 22 CVD boats, and were shown in Table 1 of after treatment.
[0020]
[Table 1]

No.	後処理内容
1	未処理（リファレンス）
2	ウエハ積載面を既存の治具（ダイヤモンド）で機械加工実施
3	ウエハ積載面を高純度SiC治具で加工実施
4	No.2処理後、ボートの超音波洗浄実施
5	No.2処理後、ボートの煮沸洗浄実施
6	No.2処理後、ボートのフッ酸洗浄実施
7	No.3処理後、ボートの超音波洗浄実施
8	No.3処理後、ボートの煮沸洗浄実施
9	No.3処理後、ボートのフッ酸洗浄実施
10	No.2処理後、ボートを酸素気流中で熱処理し、更にフッ酸洗浄実施
11	No.3処理後、ボートを酸素気流中で熱処理し、更にフッ酸洗浄実施

(notes: -- No.11 are equivalent to this invention article)
[0021] First, it destroyed one set each first and the adhesion situation of Rmax. of a wafer loading side and particle (0.1-1 micrometer) was investigated. Rmax. was measured with the sensing-pin formula surface roughness plan (Tokyo Seimitsu : SURFCOM), and the adhesion situation of particle was observed with the electron microscope (SEM). The result was shown in Table 2. In addition, the measurement conditions of Rmax. in this case were made into measurement length:10mm, cut-off value:0.8mm, scan speed:0.3 mm/sec, and repeat measurement count:10 time. It was checked that the No.1 (example of comparison) average has little boat No.11 by which Rmax. is equivalent to this invention although dispersion was accepted a little by floor to floor time etc. also as for the particle to which Rmax. has changed and adhered in the low value.
[0022]
[Table 2]

No.	Rmax.(μm)	パーティクルの付着状況（ヶ/mm^2）
1	8.0~35.0	0~ 5
2	5.5~12.2	100以上
3	5.8~13.5	100以上
4	2.2~ 7.8	100以上
5	2.3~ 7.7	100以上
6	2.1~ 7.9	100以上
7	3.6~ 9.0	100以上
8	3.7~ 8.9	100以上
9	3.5~ 9.2	100以上
10	2.0~ 7.2	20~80
11	3.2~ 8.1	0~ 4

(notes: -- No.11 are equivalent to this invention article)
[0023] Moreover, the detailed measurement result containing the survey data of Rmax. of each time about the aforementioned No.1 (example of comparison) and boat No.11 equivalent to this invention is shown in Table 3. In addition, the unit of measurement data shown in Table 3 is mum. The example of comparison is 10 micrometers or less in any or value 10 times in this invention article to the thing exceeding 10 micrometers having been 6 times in Rmax. among ten measurement, and it is clear whether "average +3sigma's" the front face is smooth equally extremely by 10 micrometers or less so that clearly from Table 3.
[0024]
[Table 3]

測定数	比較例 (No.1)	本発明 (No.11)
1	9.5	7.2
2	12.4	5.7
3	35.0	5.4
4	8.0	3.2
5	21.7	6.5
6	10.4	5.6
7	11.2	4.9
8	9.3	8.1
9	29.2	4.6
10	8.8	4.3
平均値	15.55	5.55
標準偏差	9.64	1.44
平均値+3σ	44.46	9.86
最小値	8.0	3.2
最大値	35.0	8.1

[0025] Subsequently, it is ******** about heat treatment of the conditions (inside of 1100 degrees C and an oxygen air current, 5 hours) which loaded the wafer into the non-destroying CVD boat and

assumed oxidization and the diffusion process. About the completion wafer of heat treatment, it is the impure amount of resources (MCL) of the generating situation ** wafer front face of ** slip.
** It investigated about the particle adhesion situation on the front face of a wafer.
The particle counter measurement using dispersion of light estimated the impurity analysis aforementioned ** in the oxide film by which the **** observation aforementioned ** of a wafer side was formed in the wafer front face for the aforementioned **.
The result was summarized in Table 4. In addition, the addition slip length in the table 4 showing the generating situation of a slip is a value adding all the slip length that exists in the field of one wafer. As compared with No.1 (example of comparison), that the good result more than equivalent was obtained in all items is only No.11 (this invention article) which carried out fluoric acid washing after using the SiC fixture with few impurities and passing through heat treatment in an oxygen air current, and it is ******.

[0026]
[Table 4]

No.	積算スリップ長	MCL : Fe	パーティクル数
	(mm／ウエハ)	(×10^{10}atoms／cm^2)	(ヶ／ウエハ)
1	100~140	1.0	0~10
2	60~ 90	25.0	25~40
3	65~ 95	2.0	20~35
4	15~ 25	18.0	20~35
5	15~ 25	17.0	20~35
6	15~ 25	11.0	20~35
7	20~ 30	1.8	15~30
8	20~ 30	1.6	15~30
9	20~ 30	1.3	15~30
10	5~ 20	7.0	10~25
11	5~ 25	0.9	0~ 5

(notes: -- No.11 are equivalent to this invention article)
[0027] Here, the example of a SiC fixture, the heat treatment conditions in the inside of an oxygen air current, and the washing conditions in the inside of HF solution is shown. Like the above, a SiC fixture forms a CVD-SiC film in the base which consists of Si-SiC etc., and that [its] whose maximum surface roughness is about 20-100 micrometers is desirable. since the SiC material obtained except CVD contains an impurity as an assistant or adhesives -- unsuitable -- the maximum surface roughness -- the above -- it becomes impossible for processing efficiency to fall that it is out of range, or to attain predetermined field granularity This [need / to be at least 1100 degrees C or more / the heat treatment conditions in the inside of an oxygen air current] is for advancing said reaction formula (** 1) efficiently. Generally, the reaction advance degree in the aforementioned reaction formula (** 1) is proportional to the square root of the processing time while being the function of temperature (parabola rule).
[0028] If it carries out based on this and the processing time will be set up in 15 hours in the case of 1250 degrees C, all SiC particle 1 micrometer or less will be SiO2. It will convert. Particle 1 micrometers or more is SiO2 since it is hard to stick to a front face. It is not necessary to make it turn. It is few and especially the factor that controls HF washing severely is immersing ****** SiO2 about a 2-hour or more CVD boat to 10% or more of solution. Dissolving particle completely was checked.
[0029] In addition, it sets in the gestalt and example of the above operation, and is SiO2. Although explained based on the example using fluoric acid as a dissolving solution, even if it used the mixed acid

of fluoric acid, a hydrochloric acid and fluoric acid, a nitric acid and fluoric acid, or a sulfuric acid, it was checked as the aforementioned solution that an equivalent cleaning effect is obtained. Moreover, when the content metal impure amount of resources accomplished said fixture of the quality of CVD-SiC to 0.1 ppm or less, it was also checked that the degree which generates a defect to a wafer with a metal impurity at elevated-temperature heat treatment processes, such as oxidization of a wafer and diffusion, can fall.

[0030] Moreover, in drawing 1 , although the vertical-mold wafer boat equipped with two or more wafers support board between the roof and the batholith as a fixture for semiconductors is illustrated, this invention of it being applicable to the general wafer boat equipped with the wafer retention groove such to not only a vertical-mold wafer boat [****] but to four supports is natural. Furthermore, this invention can also be applied to the susceptor of single wafer processing, the tray for wafer conveyance, etc., and can be applied to fixtures for semiconductors, such as the other reactor core tube.

[0031]

[Effect of the Invention] As mentioned above, according to the fixture for semiconductors concerning this invention, and its manufacture method Form a SiC film in a base front face by CVD, smooth this SiC film with the polishing fixture in which the SiC film was formed, and since it was made to perform particle removal by the combination of washing, such as high-temperature-oxidation processing and HF, continuously It enables it for smoothing 10 micrometers or less of the maximum surface roughness to become-possible, and to also suppress impurity contamination and particle generating. Therefore, by applying this to processing of the wafer loading side of a vertical-mold wafer boat, generating of a slip of the wafer which had become a problem conventionally can be suppressed, and it can contribute to the improvement in the yield of a processing wafer. In addition, in the fixture for semiconductors which does not contact a wafer and directly like the reactor core tube mentioned above, although there is none of said slip suppression functions, it can contribute to the improvement in the yield of a processing by the suppression function of impurity contamination or particle generating.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] At the diffusion process in a semiconductor manufacturing process, a heat treating furnace is used and hot heat treatment is made to a semiconductor wafer. In this case, as everyone knows, a semiconductor wafer is contained in the reactor core tube which consists of high grade quartz glass etc. in the form laid in the wafer boat, introduces the gas for heat treatment in a reactor core tube, and predetermined heat treatment is performed to a wafer. On the other hand, diameter-ization of macrostomia of a wafer is progressing with high integration of a semiconductor in recent years, and it has become the trend for which a vertical-mold wafer boat is used in connection with this. However, a slot is formed in a support, and when the vertical-mold wafer boat of the form which supports the edge of a wafer in this slot is used, it is the cause of generating the crystal defect which a deflection occurs in itself by the self-weight of a wafer, or the temperature gradient within a field, originates in this, and is called slip to a wafer.

[0003] Then, the wafer loading side of a wafer boat is formed in a plane, and the vertical-mold wafer boat which prevented generating of a slip to a wafer which described the wafer above as carried out field support is proposed. By the way, in such a vertical-mold wafer boat, although the quartz-glass quality of the material was conventionally used for the material, the quality of reaction-sintering SiC has come to be used from the reasons of that high grade-ization can be attained, excelling in thermal resistance by covering a SiC film with the CVD (chemical vapor dposition) method to a base in these days (CVD-SiC being called below.).

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, according to the fixture for semiconductors concerning this invention, and its manufacture method, it is. A SiC film is formed in a base front face by CVD, and this SiC film is smoothed with the polishing fixture in which the SiC film was formed, and since it was made to perform particle removal by the combination of washing, such as high-temperature-oxidation processing and HF, continuously, it enables it for smoothing 10 micrometers or less of the maximum surface roughness to become possible, and to also suppress impurity contamination and particle generating. Therefore, by applying this to processing of the wafer loading side of a vertical-mold wafer boat, generating of a slip of the wafer which had become a problem conventionally can be suppressed, and it can contribute to the improvement in the yield of a processing wafer. In addition, in the fixture for semiconductors which does not contact a wafer and directly like the reactor core tube mentioned above, although there is none of said slip suppression functions, it can contribute to the improvement in the yield of a processing wafer by the suppression function of impurity contamination or particle generating.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the following technical technical problems exist in the vertical-mold wafer boat (this is called a CVD boat below) of the quality of reaction-sintering SiC which covered the CVD-SiC film. A CVD-SiC film is first formed in the 1st of gaseous phase reaction. Under the present circumstances, unusual growth of the SiC particle in the inside of a gaseous phase is nonavoidable 100%, and some particles of them deposit on the wafer loading side of a CVD boat, and serve as an unusual salient in respect of the loading concerned. The dust which floats in a CVD coil, and a particle adhere a CVD reaction front and into a reaction in the wafer loading side of a CVD boat, a SiC film is alternatively formed in them, and it is set to the 2nd with an unusual salient in respect of the loading concerned. If CVD conditions which avoid generation of an unusual salient as much as possible are chosen as the 3rd, the crystal which constitutes a CVD-SiC film will turn big and rough, and surface irregularity will become remarkable.
[0005] In the rear face of a wafer, it is known with the unusual salient or irregularity generated by many of said factors in a wafer loading side that the defect called a slip will occur. Especially generating of the aforementioned slip is remarkable at elevated-temperature heat treatment processes, such as oxidization and diffusion, and becomes the greatest factor which reduces the yield of a heat treatment wafer. According to artificers' experiment measurement, it was checked that the slip generated to a wafer in the situation that maximum surface roughness Rmax. exceeds 10 micrometers by n aforementioned measurement, in the measurement of Lxn>=100mm in the surface roughness measurement at the time of being referred to as measurement length:Lmm and measurement count:n increases extremely. It is thought that this is to field-support not but point support a wafer substantially in a loading side, and for an excessive load to concentrate on a wafer side in the aforementioned point supporter in the rear-face section of a wafer.
[0006] Then, although artificers examined how to machine the wafer loading side covered with the CVD film by the diamond wheel etc., and smooth etc. as the technique of reducing Rmax. of a wafer loading side The technical technical problem that processing it with such a fixture generated a defect to a wafer at elevated-temperature heat treatment processes, such as oxidization of the wafer which the impurity contamination from the fixture for machining generated and described above, and diffusion, occurred. Furthermore, the particle 1 micrometer or less generated at the time of processing stuck to the wafer loading side, it became a source of particle within a process, and the technical technical problem that the yield of the wafer in the time of heat treatment will be lowered in another meaning occurred.
[0007] It is made in order that this invention may solve a technical technical problem which was described above, and the influence of the impurity contamination to a wafer is lost, and it aims at offering the fixture for semiconductors which may improve the yield of a wafer based on impurity contamination, and its manufacture method. Moreover, this invention aims at offering the vertical-mold wafer boat which improves the smoothness in a wafer loading side, and reduces generating of a slip to a wafer, and may improve the processing efficiency of flat-surface processing of a wafer loading side, and its manufacture method, when a wafer loading side is applied to the vertical-mold wafer boat made into the plane.

[Translation done.]